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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,736	09/28/2001	Mark E. Eidson	2207/11983	2175

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,736	EIDSON, MARK E.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani et al.('076), hereinafter referred to as Fadavi-Ardekani.

3. Regarding claim 1, Fadavi-Ardekani discloses a system comprising: a plurality of memory bus masters(Figure 1, 300, 102, 104, 106), each to generate an independent clock signal on respective outputs, each of said outputs connected by a transmission line(Figure 1, Agents' clock signals) to a common node(Figure 1, 130), said common node additionally connected to a plurality of clock inputs of a memory array(Column 4, Lines 27-28); and an isolation circuit(Figure 1, 110 and 118 combined) coupled between each of said transmission lines and said common node, the isolation circuit including a switching device coupled to a respective transmission line and a corresponding respective control input(Figure 1, 114), the respective control input to select or de-select the respective transmission line for input to the memory array(Column 4, Lines 54-67; One transmission line is selected and the others are de-selected).

4. Regarding claim 2, Fadavi-Ardekani discloses a system, wherein the control inputs select one of said plurality of memory bus masters to drive a corresponding clock signal to said

memory array while isolating the transmission lines of the other bus masters from said common node(Column 4, Lines 54-67).

5. Regarding claim 3, Fadavi-Ardekani discloses a system, wherein said control inputs are supplied by a memory bus arbiter(Figure 1,112).

6. Regarding claim 4, Fadavi-Ardekani discloses a system, wherein said isolation circuit places a high impedance between said common node and said transmission lines(Column 4, Lines 54-67; Only one clock input is selected and therefore introducing high impedance to the non-selected clock inputs).

7. Regarding claim 5, Fadavi-Ardekani discloses a system, wherein said isolation circuit comprises a plurality of FETs(It is inherent for the isolation circuit to comprise a plurality of FETs).

8. Regarding claim 6, Fadavi-Ardekani discloses a system, wherein said isolation circuit is a multiplexer(Figure 1, 118).

9. Regarding claim 7, Fadavi-Ardekani discloses a computer board layout including a memory array(Figure 1, 302) and plurality of memory bus masters(Figure 1, 300, 102, 104, 106), a method comprising: connecting each of said bus masters to a common node((Figure 1, 130) via a transmission line(Figure 1, Agents' clock signals); connecting said memory array to said common node; and placing an isolation circuit(Figure 1, 112 and118 combined) between each of said transmission lines and said common node; in the isolation circuit, pairing each of the transmission lines with a corresponding respective control input(Figure 1, 114), to select one of said bus masters to drive a clock input to said memory array while isolating the transmission lines of the other bus masters from said common node(Column 4, Lines 54-67; One bus master is selected to drive the clock input of the memory and the other bus masters' transmission lines are isolated).

10. Regarding claim 9, Fadavi-Ardekani discloses a circuit comprising: a plurality of transmission lines(Figure 1, Agents' clock signals) coupled between respective bus master clock outputs(Figure 1, 300, 102, 104, 106) and a common node(Figure 1, 130); a plurality of memory modules(Figure 1, 302; Column 4, Lines 27-28; Plurality clock signals indicate plurality memory modules) coupled to said common node; and an isolation circuit (Figure 1, 112 and 118 combined) coupled between said plurality of transmission lines and said common node, the isolation circuit including a switching device coupled to a respective transmission line and a corresponding respective control input(Figure 1, 114), the respective control input to select or de-select the respective transmission line for input to the memory modules(Column 4, Lines 54-67; One transmission line is selected and the others are de-selected).

11. Regarding claim 10, Fadavi-Ardekani discloses a circuit, further comprising: bus arbiter means(Figure 1, 112) to determine values of the control inputs to select one of said bus master clock outputs to drive to said memory modules, while selecting the transmission lines associated with the other bus master clock signals for isolation from said common node(Column 4, Lines 54-67).

12. Regarding claim 11, Fadavi-Ardekani discloses a circuit, wherein a clock input of each of said memory modules is connected to said common node(Figure 1).

13. Regarding claim 12, Fadavi-Ardekani discloses a circuit, where said memory modules are SDRAM modules(Column 3, Lines 38-39).

14. Regarding claim 13, Fadavi-Ardekani discloses a method comprising: connecting transmission lines(Figure 1, Agents' clock signals) from a plurality of memory bus masters(Figure 1, 300, 102, 104, 106) to a common node(Figure 1, 130); connecting a memory array(Figure 1, 302) to said common node; pairing each of the transmission lines with a corresponding respective control input(Figure 1, 114) to select one of said bus masters to drive

a clock input to said memory array while isolating the transmission lines of the other bus masters from said common node selecting one of said memory bus masters to drive clock outputs to said memory array by asserting a corresponding respective control input; and introducing a high impedance between the transmission lines of the other memory bus masters and said common node by asserting the other control inputs(Column 4, Lines 54-67, Only one clock input is selected and therefore introducing high impedance to the non-selected clock inputs).

15. Regarding claim 14, Fadavi-Ardekani discloses a method, wherein said control inputs are from a memory bus arbiter(Figure 1, 112).

16. Regarding claim 15, Fadavi-Ardekani discloses a method, wherein said high impedance comprises FETs(It is inherent for the isolation circuit to comprise a plurality of FETs since they are extensively used in the industry).

Response to Arguments

17. Applicant's arguments filed July 15, 2004 have been fully considered but they are not persuasive. Applicant argues that the inactivation signal 116 does not select a clock input. However, 116 includes clock switching control signals 114 to select a clock input and de-select the other clock inputs, as stated in the above rejection.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
September 30, 2004

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100